Compact Accelerated Life Testing with Expanded Measurement Suite

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Abstract — An accelerated-life-testing (ALT) system has been built at the Colorado State University Photovoltaics Laboratory with an emphasis on versatility and periodically performing a suite of electronic measurements on stressed devices. The setup utilizes a scientific oven with a footprint of 17 X 17 inches as a stress chamber and four commercially available 40 W broad-spectrum LED arrays. A preliminary study has been performed on Cadmium Telluride (CdTe) devices. Devices were held at elevated temperature and were exposed to nominally one-sun illumination. Measurements taken of stressed devices include J-V, QE, C-V, electroluminescence (EL) and light-beam-induced current (LBIC).

Index Terms — Cadmium compounds, photovoltaic cells, stress measurement, electroluminescence, current measurement.

I. INTRODUCTION

A state-of-the-art accelerated-life-testing (ALT) system that allows cells to be exposed to elevated temperatures under illumination has been built at the Colorado State University Photovoltaics Laboratory. The system was designed with an emphasis on a compact footprint and independent control of light and temperature. The purpose of the setup is to study the stability of cells with novel structure and to investigate mechanisms responsible for degradation. A suite of electrical measurements were used including J-V, QE, C-V, EL and LBIC. The work described here demonstrates the capability of a system as applied to CdS/CdTe cells with efficiency around 10%.

II. EXPERIMENTAL SETUP

The ALT setup utilizes a Fisher Scientific, Isotemp 500 series oven as the enclosure and heat source, as shown in Figure 1. The enclosure can elevate the temperature up to 210 °C and has a footprint of 17 X 17 inches. Four apertures were added to the top of the oven, each of which has a commercially available LED array mounted over it (Bridgelux 30G10K0L). Each LED array consumes 40 W of electrical power, and in absence of proper thermal management would heat up to destructive temperatures. A computer heat sink and cooling fan is mounted to the LED array, forming an LED assembly. Each LED array emits negligible light in IR spectrum, allowing independent control of device temperature and illumination.

Devices stressed were made at CSU via their standard closed-space sublimation process [1] with a TEC 12D/120 nm CdS/2 µm CdTe/back contact structure with a CdCl₂ and copper treatment. Devices stressed had initial efficiency of ~10%. Nine devices were placed in the ALT enclosure under approximately one-sun of illumination, three were held at 60 °C under open-circuit, three devices were held at 85 °C under open-circuit and three were held at 85 °C under short-circuit. Devices were measured after nominally 0, 1, 24, 36, 72 and 144 hours of stressing. J-V measurements on three representative devices and additional electrical measurements on one of those devices are presented in this paper.

Fig. 1. Schematic of ALT setup with 5 main components: heated enclosure, LED assembly, LED power supply, devices to stress and a temperature controller.

Devices were removed from ALT enclosure and cooled to ambient for measurement. J-V curves were measured under standard test conditions. Electroluminescence (EL) images were collected periodically to help map out spatial changes in open-circuit voltage and spatially characterize change in defects. EL images are displayed on a log scale; measurement details are described in previous work [2]. Light-beam-induced current (LBIC) maps were measured on select devices with a wavelength of 638 nm and 830 nm with a spot size of 100 µm and at 0 and 0.6 V biases; measurement details are described in previous work [3]. Capacitance-Voltage (C-V)
measurements were measured at 100 kHz to investigate changes in bulk doping.

III. RESULTS

The J-V parameters in Figure 2 demonstrate device degradation occurred within the first hour of stressing and partially recovered after 24 hours. Data suggests the most severe electronic degradation occurs at elevated stress temperature and short-circuit conditions.

A device stressed at 85 °C under short-circuit conditions was used to illustrate changes induced in device from stressing, see Figure 3 for device J-V curve. Small changes in the device’s short-circuit current density are reflected as small changes in the QE curves.

Figure 4 is a plot of the device’s doping density profile measured after 0 and 144 hours of stressing. Although this device has no measurable change in bulk doping density, a more significant change in bulk doping density was measured for the device stressed at 60 °C.

EL images of the device at various stress times are displayed in Figure 5 with respective open-circuit voltages listed. The EL intensity scale listed in Figure 5 is on a log-scale and is in arbitrary units. As shown elsewhere [2], EL intensity has been found to track well with open-circuit voltage. EL images illustrate an increase in non-uniformities and reduction in EL intensity with stress time, as reflected in open-circuit voltage.

Fig. 4. Bulk doping density of CdTe cell had no measurable change after 144 hours of stressing at 85 °C and short-circuit.

Fig. 5. Electroluminescence images of CdTe device measured periodically with respective open-circuit voltage and stress time labeled. Image intensity is on a log-scale.
Figure 6 is LBIC maps of the device, measured at 0 and 144 hours of stress. Largest reduction in device QE after stressing can be seen at 0.6 V forward bias. This is also demonstrated in device J-V curve, see Figure 3. Regions in cell of poor response at 0 hours of stress exhibit further reduction after 144 hours of stress. In general, uniformity seems to get worse with increasing stress.

Although in-depth analysis of non-uniformities is outside the scope of this paper, non-uniformities which appear in EL images also appear in LBIC maps. LBIC maps have been shown to be a powerful tool in diagnosing non-uniformities [3].

IV. CONCLUSION

A state-of-the-art accelerated life testing setup has been built at the Colorado State University Photovoltaics Laboratory. The ALT system uses a scientific oven with a footprint of 17 X 17 inches and uses LED’s as a light source which emit no light in the IR. Proof of concept of ALT setup was demonstrated with stressing CdS/CdTe devices at different temperatures and electronic load. Device was periodically measured with a suite of electrical measurements. Changes were observed in J-V parameters however little changes were measured in bulk doping density. EL and LBIC measurements of device exhibited a reduction in signal after 144 hours of stressing.

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REFERENCES

